Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**BONDING PAD**

**Do not bond to back contact via**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .020” X .020” DATE: 4/27/23**

**MFG: VISHAY THICKNESS .015” P/N: WBCR-008-10000F**

**DG 10.1.2**

#### Rev B, 7/19/02